ABSTRACT

The invention relates generally to a method of power supply noise and signal integrity analysis for creating frequency-dependent electrical models particularly related to microelectronic packages. The method discloses creation of equivalent circuits for geometries encountered in a typical chip package, including how to partition the geometry into cells which are less then 1/20 the minimum wavelength (λ) in size, and how to handle signal and power supply vias, signal wires, and power planes. The method also instructs how to assign values to each of the inductors, capacitors, resistors, and transmission lines in each equivalent circuit. The method further provides modeling of only those interactions which occur between adjacent cells.